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Electromagnetic Characteristics on Interposer Through Finite Element Analysis

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Abstract: The 2.5D package is a package to which an interposer is applied to implement heterogeneous chips into one package. The core of 2.5D packaging technology is the interposer including TSV. Interposer technology with TSVs is getting a lot of attention in 2.5D packages, but 2.5D packages suffer from electromagnetic problems such as crosstalk, propagation delay, power noise, and thermal degradation. Therefore, in this study, scattering coefficient characteristics were simulated by controlling various factors of the interposer or TSV in the frequency range of 400 MHz to 20 GHz through an EM (Electromagnetic) solver, focusing on insertion loss and return loss. After modeling through AEDT (Ansys Electronics Desktop), simulations were performed for three factors: resistivity control of interposer, Cu filling factor control, and material change of Tsv center, and electrical characteristics for each simulation were analyzed.

Keywords: Interposer, FEM, S-paramter, TSV

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1. Introduction

Your goal is to simulate the usual appearance of papers in a Conference Proceedings or Journal Publications of the RAME Publishers. We are requesting that you follow these guidelines as closely as possible.In July 2015, ITRS(International Technology Roadmap for Semiconductors) suggested the direction of semiconductor R&D as 'More Moore', Beyond CMOS', and 'More than Moore'[1]. 'More Moore' refers to the direction of realizing high integration of semiconductor circuits based on Moore's Law. 'Beyond CMOS' means to the development direction for devices with operating principles other than CMOS, which is a switch device configuration method of general integrated circuits. 'More than Moore' means to the direction of improving semiconductor performance through innovation in the semiconductor back-end process. Among the three directions suggested by ITRS, 'More than Moore' suggests the need for semiconductor back-end process technology development. Currently, in the semiconductor industry, development of back-end process technologies such as FOWLP (Fan-out Wafer Level Package), Interposer, Hybrid Bonding, and EMIB (embedded multi-die interconnect bridge) is actively progressing[2-4]. According to the roadmap presented by HIR (Heterogeneous Integration Roadmap) in 2021, packaging technology is predicted to develop into a 2.5D/3D package capable of realizing high integration and high performance through the stacking of heterogeneous chips [5-7]. The 2.5D package refers to a package to which an interposer is applied to implement heterogeneous chips into a single package. Major processor developers are using 2.5D packaging technology that stacks CPU/GPU and HBM(High Bandwidth Memory) through an interposer such as Intel's Foveros, Samsung's I-cube, and AMD's X3D. The core of 2.5D package technology is an interposer that includes Through Silicon Via (TSV). Since the top and bottom are connected vertically through the TSV of the interposer, the length of the communication channel is shortened, and a small form factor can be implemented, thereby reducing power consumption [8]. However, electromagnetic problems such as crosstalk, propagation delay, power noise, and thermal performance degradation due to the narrowing spacing and wiring width of TSVs are still emerging [8-11]. In addition, high-performance devices that require high data processing speed, such as HBM, suffer greatly from performance degradation due to electromagnetic problems [12-13].

In response to these problems, research on electromagnetic wave issues such as channel characteristics study according to interposer substrate material, crosstalk study according to wiring interval, PI/SI study occurring in interposer RDL (Redistribution Layer), and electromagnetic wave effect study according to TSV design A variety of studies are being conducted [8,12,14]. In particular, studies through computational simulation based on FEM (Finite Element Method) are being actively conducted to identify electromagnetic problems [6,7,13,14]. The advantage of simulation is that time and cost can be saved because there is no need to manufacture actual semiconductors, and results can be confirmed by easily applying various variables. In this study, based on the EM (Electromagnetic) solver and FEM, the electrical characteristics were analyzed by conducting simulations according to the resistivity of the silicon interposer, the Cu filling rate inside the TSV, and the material of the TSV center filler.

2. Interposer Model

For simulation, modeling was performed as shown in Figure 1. The model was made through AEDT (Ansys Electronics Desktop), and the physical properties and size are shown in Table 1. Ansys HFSS tool was used to analyze the electrical characteristics of this model. HFSS performs analysis based on FEA (Finite Element Analysis). The analysis was conducted with S-parameters extracted by simulation, such as the resistivity of the interposer through the electromagnetic field, the Cu filling rate inside the TSV, and the TSV center filler.

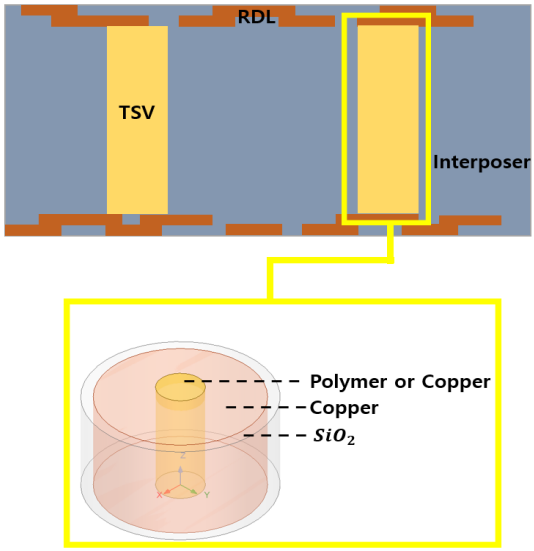

Figure 1. Simplified interposer model.

Table 1. Size and Properties of the FEM Model

	Size(um)	Thickness(um)	Material
TSV	11(diameter)	33	Cu
SiO_2	1.5	33	SiO_2
Polymer	1	33	Polymer
Passivation	300 x 300	2	Polymer

2.1 Electrical Characteristics by Adjusting Interposer's Resistivity

Interposer insertion loss characteristics at high frequencies are important for memories that require high performance. In a previous study (Masahiro Sunohara et al., 2010.), to reduce the loss of the Si interposer, a Si interposer with resistance characteristics of 1 ~ 800 Ohm·cm was fabricated and the results were analyzed. As a result, it was shown that the higher the Si resistance, the more the insertion loss generated by the TSV is reduced [15]. Similarly, in this study, the resistance characteristics of Si were varied to confirm the tendency and the results were compared using Ansys HFSS. In the simulation, it was possible to directly apply various variables and observe the results without a time limit, compared to making samples and checking the results. Therefore, analysis was performed as shown in Fig. 2 and Fig. 3 with various resistance values ranging from 1 to 800 Ohm·cm. We observed better than scattering coefficient characteristics of the Si interposer with a relatively low resistivity of 800 Ohm cm. In addition, the interposer with a resistance value of 15

Ohm·cm showed the best reflection coefficient characteristics from 400 MHz to 20 GHz. For values larger than 100 Ohm·cm, the characteristics of the reflection coefficient tended to converge to a specific value. In addition, the insertion loss decreases as the Si resistance increases. Therefore, it was confirmed that the insertion loss increased rapidly at the resistance value of 1 Ohm·cm, which is the smallest resistance value in the simulation. In addition, since there are wafers with a resistivity of 0.01-100 ohm [16], based on these results, rapid loss is expected at a resistance level of less than 1 Ohm cm, so it is a substrate for semiconductors requiring high performance, with a resistivity of less than 1 Ohm cm. It was concluded that applying wafers was not appropriate.

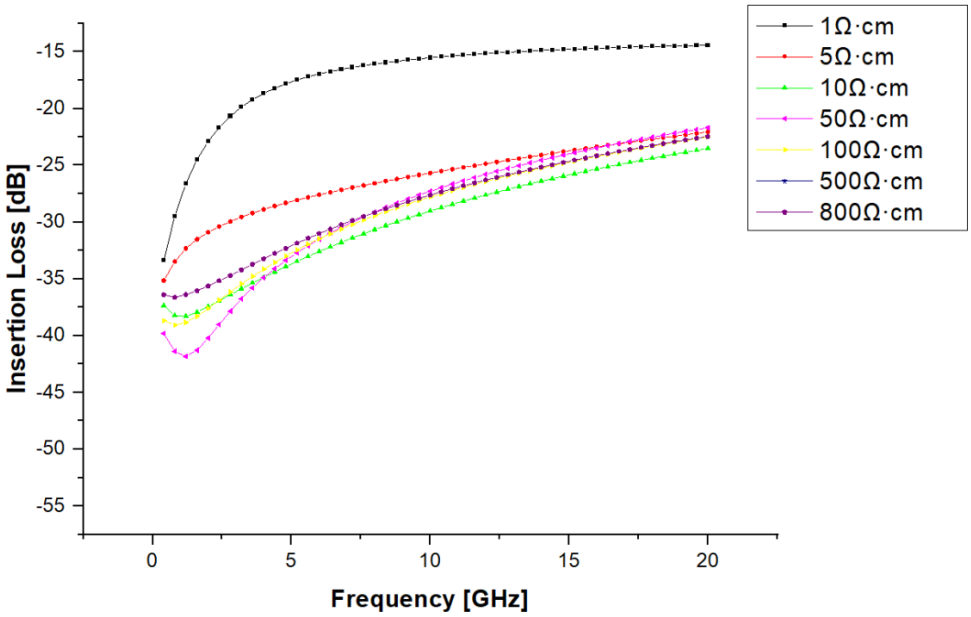

Figure 2. Return loss graph obtained by adjusting the resistivity of Si.

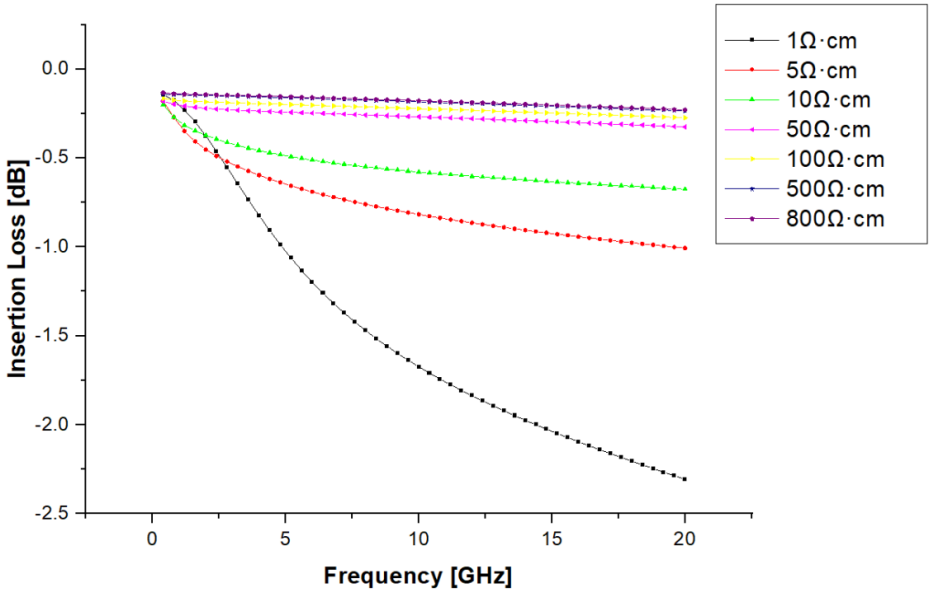

Figure 3. Insertion loss graph obtained by adjusting the resistivity of Si.

2.2 Electrical Characteristics according to Cu filling rate inside TSV

The inside of the TSV of the interposer is filled with Cu after forming the SiO2 thin film. SiO2 prevents diffusion of Cu into the interposer substrate during Cu charging. In some cases, Cu, which is an electrical path, is completely filled inside the TSV. In other cases, Cu is formed only on the side walls and the center may or may not be filled with polymer. Therefore, it was expected that the electrical characteristics would change according to the TSV filling area of Cu, and the S-parameter was confirmed by changing the filling factor of the sidewall from 20% to 100%. As a result, the insertion loss decreased as the Cu filling area increased within the 11um diameter range, which is the TSV size design rule of the HBM interposer manufactured in the field. However, changes in S-parameter characteristics were effective within the range of about 2.5 GHz. After about 2.5 GHz, there was a slight trend.

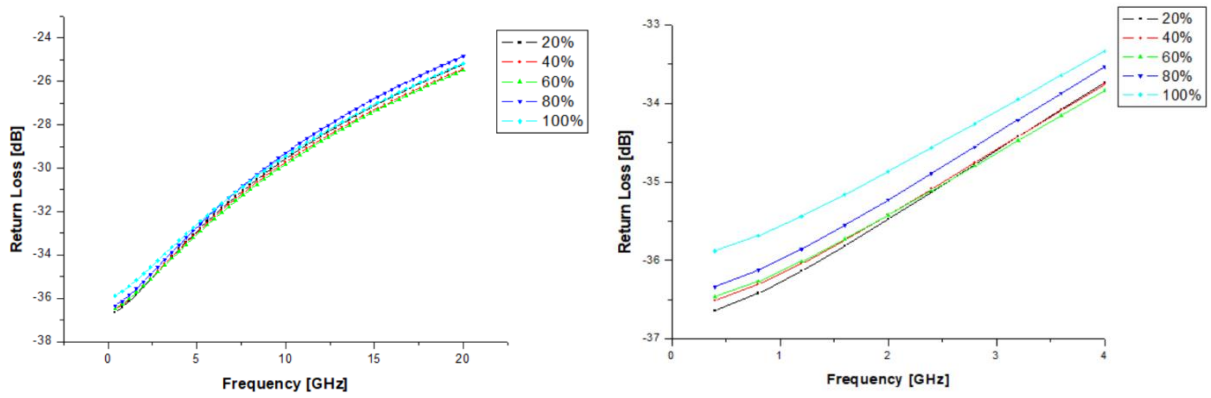

Figure 4. Return loss according to sidewall Cu filling ratio of TSV(Left: from 400MHz to 20GHz, Right: from 400MHz to 4GHz)

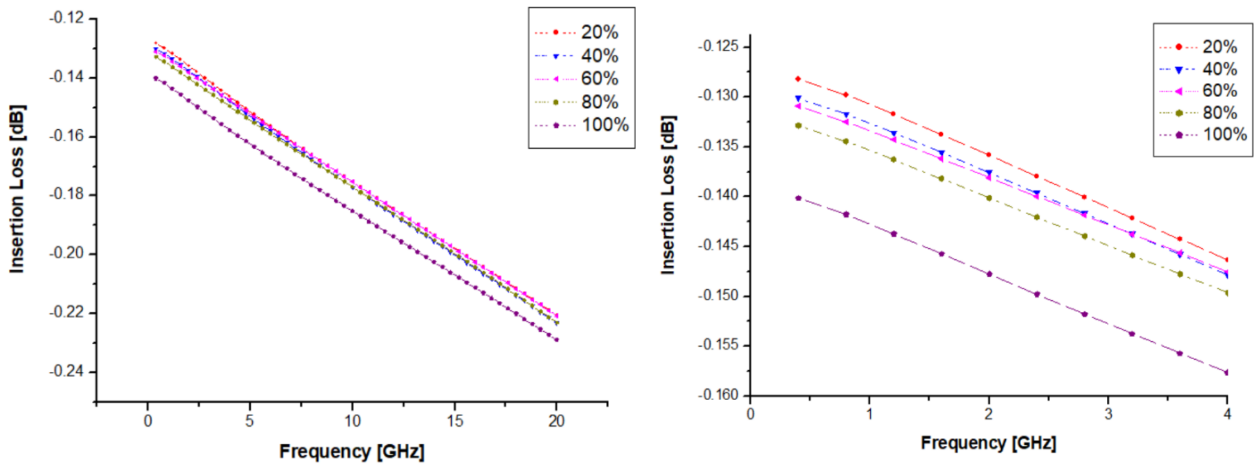

Figure 5. Insertion loss according to sidewall Cu filling ratio of TSV(Left: from 400MHz to 20GHz, Right: from 400MHz to 4GHz)

2.3 Electrical Properties according to TSV center filler

The effect of the TSV filling factor on the electrical properties was confirmed to be insignificant, so a model in which only 50% of the TSV sidewall was filled with Cu was used. In the empty center of TSV, the filling materials were changed to Air, Polymer and Cu. After that, the effect of the electrical properties on the material deformation of the TSV center filler was confirmed. As a result, Fig. As shown in Fig. 6, the insertion loss characteristics according to the filler change of the TSV center were similar for air, polymer, and Cu materials within the frequency range of 400 MHz to 20 GHz.

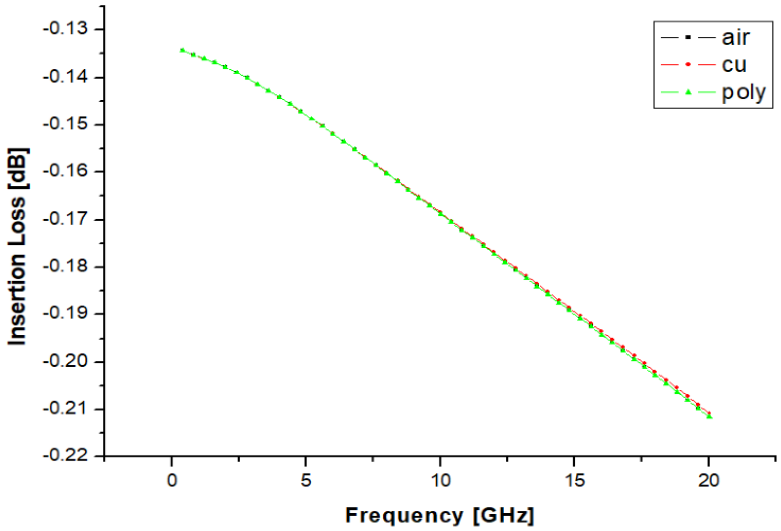

Figure 6. Insertion loss according to TSV inner filler

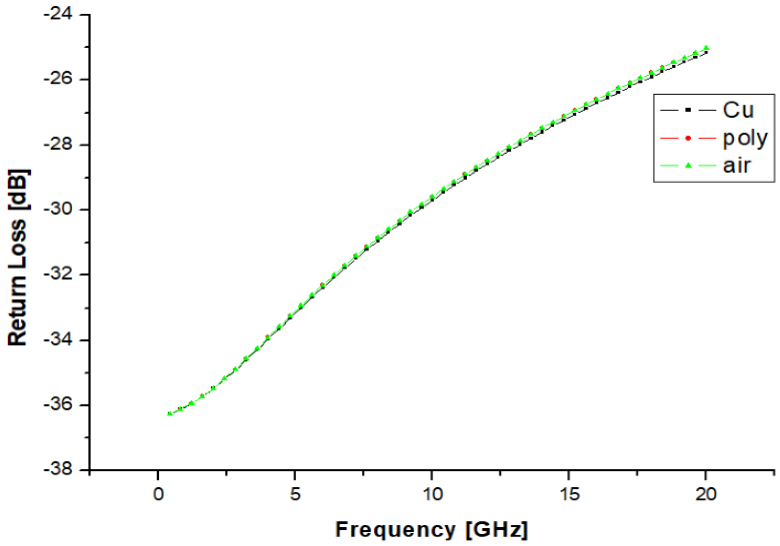

Figure 7. Insertion loss according to TSV inner filler

3. Conclusions

In this study, the electrical characteristics of the silicon interposer and TSV were simulated using an EM solver. The results of the simulation are as follows.

1) The resistivity was varied from 1 to 800 Ohm·cm to change the silicon resistivity value. As the resistance of the silicon substrate increased, the reflection coefficient and insertion loss showed a sharp drop after about 2.5 GHz. In the case of resistivity Si having a resistance of less than 1 Ohm*cm, it is determined that it is not suitable for use as a substrate material for an interposer due to rapid loss in a high frequency band.

2) The TSV Cu fill factor was changed from 20% to 100% for 11 μm TSV diameter. As the Cu filling factor of the TSVs increased, the insertion loss decreased within the range of about 2.5 GHz. However, these differences were negligible in overall losses. Therefore, it was concluded that changing the Cu filling factor of TSVs to solve the signal loss problem does not have a significant effect.

3) The scattering coefficient characteristics were observed for three cases in which the filling rate of TSV Cu was maintained at 50% and the empty part inside the TSV was filled with air, Cu, and polymer. Scattering coefficients for Air, Cu, and Polymer showed no significant difference.

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